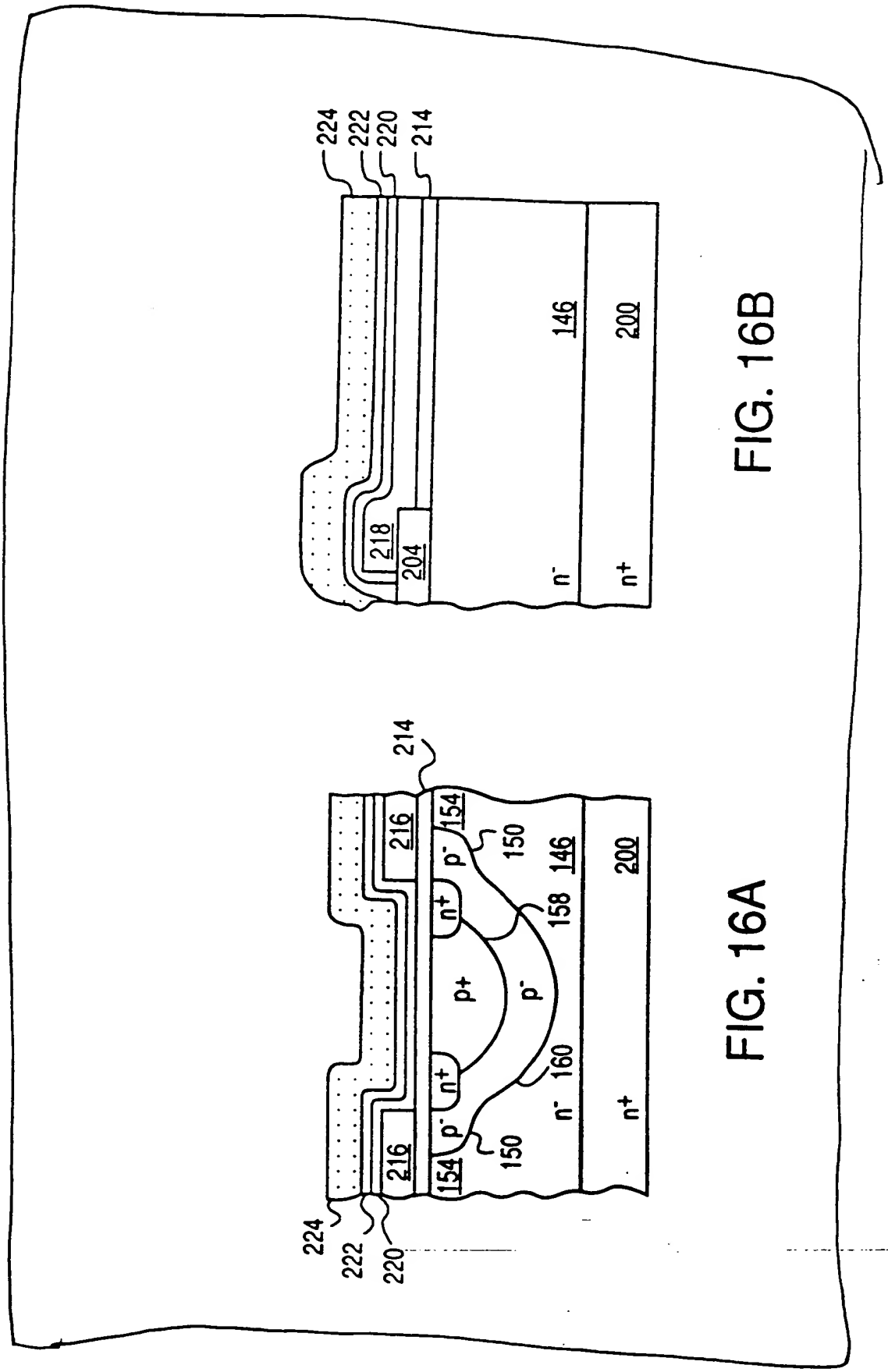


FIG. 16B

FIG. 16A

Fig. 1A (Prior Art)

suitable furnace through the window **206** at 750–1000 degrees C. A Boron rich glass **212** forms in the window **206** during the injection. A Boron soak is carried out in any suitable oven at 750–1000 degrees C. for from 15 minutes to 3 hours, as appropriate, wherein boron from the glass continues to diffuse into the epitaxial silicon to form p+ body contact **158** in the p− tub **160** (FIG. **10**). The sheet resistance of the p+ body contact is 10–100 ohms/square.

In a second masking step, the field oxide **204** is protected in the peripheral termination region, including gate finger regions. All oxide is removed from the active device areas, and gate oxide **214** is thermally grown at 900 -1100 degrees C. for 20 minutes to 3 hours, as desired (FIG. **11**).

A polysilicon film is deposited to a thickness of 0.3 -0.7 microns using any suitable equipment. A polysilicon film also is deposited on the backside, and is removed along with an underlying oxide in a wet oxide etch for the purpose of exposing the wafer backside to heavy diffusion using phosphorus or other suitable dopant. The polysilicon film is then doped to less than about 20 ohm/square, and is patterned in a third masking step for opening windows to form p− body, n+ source regions, and ultimately metal contacts to the source and body. The polysilicon film is etched in any suitable equipment to form gate poly **216** and periphery strip **218**, a component of a termination structure. The resist is stripped, and Boron is implanted at a dose of 5E13–2E14 ions/cm^2 and an energy of 40–100 KeV in any suitable equipment (FIG. **13**). The Boron is diffused at 900–1200 degrees C. for 10 minutes to 5 hours, as desired. The purpose of this diffusion is to form the double diffused channel **144** as shown in FIGS. **5** and **6**.

Oxide is etched from the p− body diffusion region using either a dry or wet etch, as desired, and a layer of suitable photoresist is deposited and patterned in a fourth masking step to form a sound mask (FIG. **14**). An Arsenic implant is made using a dose of 1E15–1E16 ions/cm^2 at an energy of 60–120 KeV, after which the resist is stripped (FIG. **15**) and the Arsenic diffused at 850–1100 degrees C. for 0.5–1 hour to form the annular square source region **152** with blunted corners. An oxide layer **220** forms during the Arsenic diffusion (FIG. **16**). The annular square channel **144** with blunted corners is defined in the body **158** between the source region **152** and the drain **154**. Again, see FIGS. **5** and **6**. At this point, the junction profile of the cell is essentially established.

The device is completed by depositing (optionally) about 1000 Angstroms of LPCVD nitride **222** followed by a BPSG deposition of about 0.8–1.3 microns and a BPSG reflow **224** at about 850–1000 degrees C. (FIG. **16**). The fifth masking step is a contact mask, which defines the source-body contact and the poly gate contact. The BPSG layer **224**, the nitride layer **222**, and the oxide layer **220** are suitably etched in a sequence involving, for example, a descum, a dry etch in suitable equipment, and a resist strip, followed by a reflow of the BPSG at 850–1100 degrees C. for 10–30 minutes (FIG. **17**). A suitable metal such as aluminum or a material such as aluminum with 1 percent silicon is deposited using, for example, sputter deposition, and is suitably patterned in a sixth masking step and etched to form the source electrode **226**, the gate electrode (not shown), and termination field plates (not shown). Films of PSG **228** and/or plasma nitride **230** are deposited, pad contact holes are opened in a seventh masking step, and an alloy step is performed at 300–450 degrees C. in an inert ambient.

The termination structure **234** comprising field oxide **204**, gate oxide **214**, and polysilicon periphery strip **218** need only be coupled electrostatically to the epitaxial silicon **146** in order to function satisfactorily. The coupling is achieved when the die is separated from the wafer by dicing, since the thin gate oxide **214** near the die edge is damaged and becomes leaky. The termination structure **234** assumes the voltage level of the epitaxial layer **146**, and at this potential acts to exclude the depletion region from the leaky damaged silicon at the die edge.

FIG. **18A** shows one embodiment of the full termination structure **234**, including a typical inactive cell **300**. The inactive cell **300** is similar to the active cells except no channel region is provided, although a p− tub **302** and p+ body contact **304** are provided. Source metal **306** shorts a polysilicon ring **308** and the inactive cell **300** to the source electrode. FIG. **18B** shows another embodiment of the full termination structure **234** wherein all portions of polysilicon ring **308** are separated from the underlying semiconductor body by field oxide **204**.

FIG. **19** shows a plan view of a completed device with the gate fingers **320***a*–**320***e*, gate bonding pad **322**, source metal **324**, and source bonding pad **326**. The exploded view of FIG. **20** shows the juxtaposition of the active cells **330***a*–**330***d* (other active cells in the device are not shown), the inactive cells **332***a*–**332***d* (other inactive cells in the device are not shown), the gate finger **320***e*, and the p+ polysilicon ring **334**.

These techniques have been used to achieve a specific on-resistance of 1.65 milliohms-cm^2 for 60 volt devices, and 0.85 milliohms-cm^2 for 30 volt devices.

As will be recognized, six masking steps are utilized in an alternative embodiment of the fabrication process described in FIGS. **7A–20** of the present invention. These six masking steps are as follows:

1) a deep P+ masking step in which an opening is formed in layer **204** as shown in FIG. **8A** through which a P+ implant is performed;

2) a masking step in which a portion of photoresist is formed to protect and thereby to form the portion of oxide layer **204** shown in FIG. **11B**;

3) a polysilicon masking step in which portions of photoresist are used to protect and thereby to form the portions of polysilicon layers **216** and **218** shown in FIGS. **12A** and **12B**;

4) a contact masking step in which portions of BPSG layer **224** are removed to form a contact to P+ region **158** of FIG. **17A**, to form a contact to P+ region **304** of FIG. **18A**, and to form a contact to poly region **308** of FIG. **18A**;

5) a metal masking step in which portions of a metal layer **226** are removed to form the metal source electrode **226** of FIG. **17A**, the metal gate finger of FIG. **18A**, and the termination metal **306** of FIG. **18A**; and

6) a pad masking step in which portions of layer **228** and/or **230** are removed to expose portions of gate bonding pad **322** and source bonding pad **326** of FIG. **19**.

Another embodiment of the present invention will now be described. This embodiment, hereafter referred to as one embodiment of a five masking step process, requires only five masking steps to fabricate a DMOSFET device, such as a vertical DMOSFET, and an associated termination structure. FIGS. **21A–21M** show

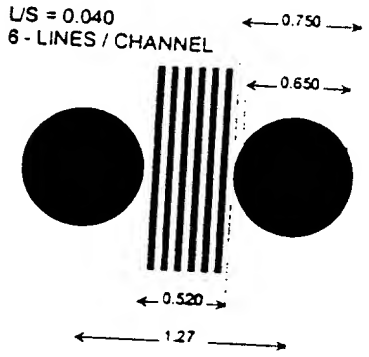
Fig. 1B (Prior Art)

The primary advantage of the flex substrate is the high density of routing. As shown in figure 9, up to seven rows of solder balls at 1.27mm pitch can be routed using 40μm lines and spaces with 0.75mm solder ball and 0.65mm diameter solder mask defined pad. Table I shows that the routing capability of the flex substrate far exceeds the routing capability of multilayer PCBs today down to 0.5mm pitch solder balls.

The minimum lines and spaces allowed on the one-metal flex substrate are 30μm with 12-18μm thick copper and on the two-metal are 50μm with 15μm thick copper layers connected with 50μm copper filled vias.

All the plating tales are bussed to the central device window which is subsequently punched out. This reduces the routing density and eliminates the plating tales that can cause electrical noise at high operating frequencies.

The location of the ground vias on the substrate can be assigned as needed without appreciably affecting the inductance of the connection. The outer row of solder balls is usually the hardest to route and has the longest traces therefore it is advantageous to the overall performance to assign the ground to the outer row of solder balls including the corners and eliminate the routes.



1418

Fig 9 S-TBGA flex substrate routing . All dimensions in mm.

the distance between the cavity and the inner row of solder balls competes for the same space as the cavity for a given package. The finer routing pitch on the flex substrate minimizes the fan out length and reduces the distance from the die edge to the inner-most row of solder balls to 2.2mm.

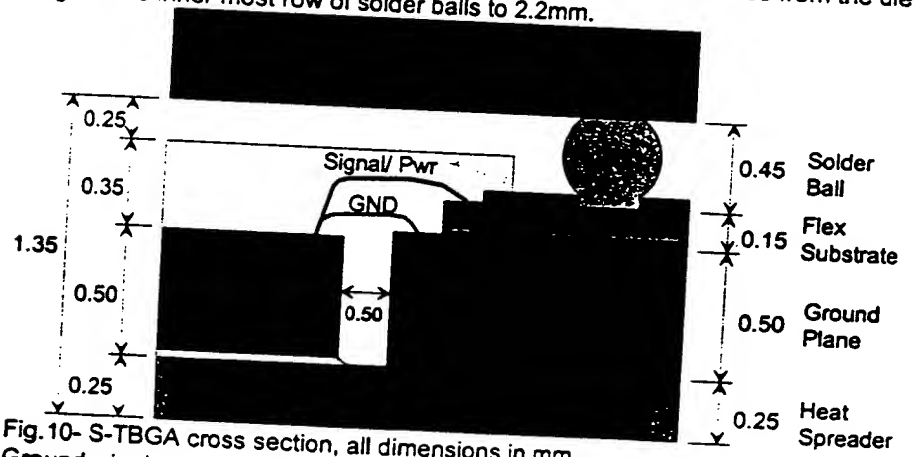


Fig.10- S-TBGA cross section, all dimensions in mm.
Ground wire length =0.75mm, signal/power bond wire length =1.2mm.

Finer pitch on the substrate allows finer pad pitch on the die without having to use long wires. It is known that the maximum number of in-line pads possible to bond with the finest pitch on each side of the die, depend on the bond finger pitch and wire length, assuming the angle between the wire and the die edge is no less than 45° degrees. Starting with 80μm pad pitch at the center of the die and decreasing the finger pitch from 180μm possible on a PCB substrate to 125μm easily achieved on the flex substrate it allows 3X more bonding-pads-at a

1420

Fig. 1 c. (PRIOR ART)

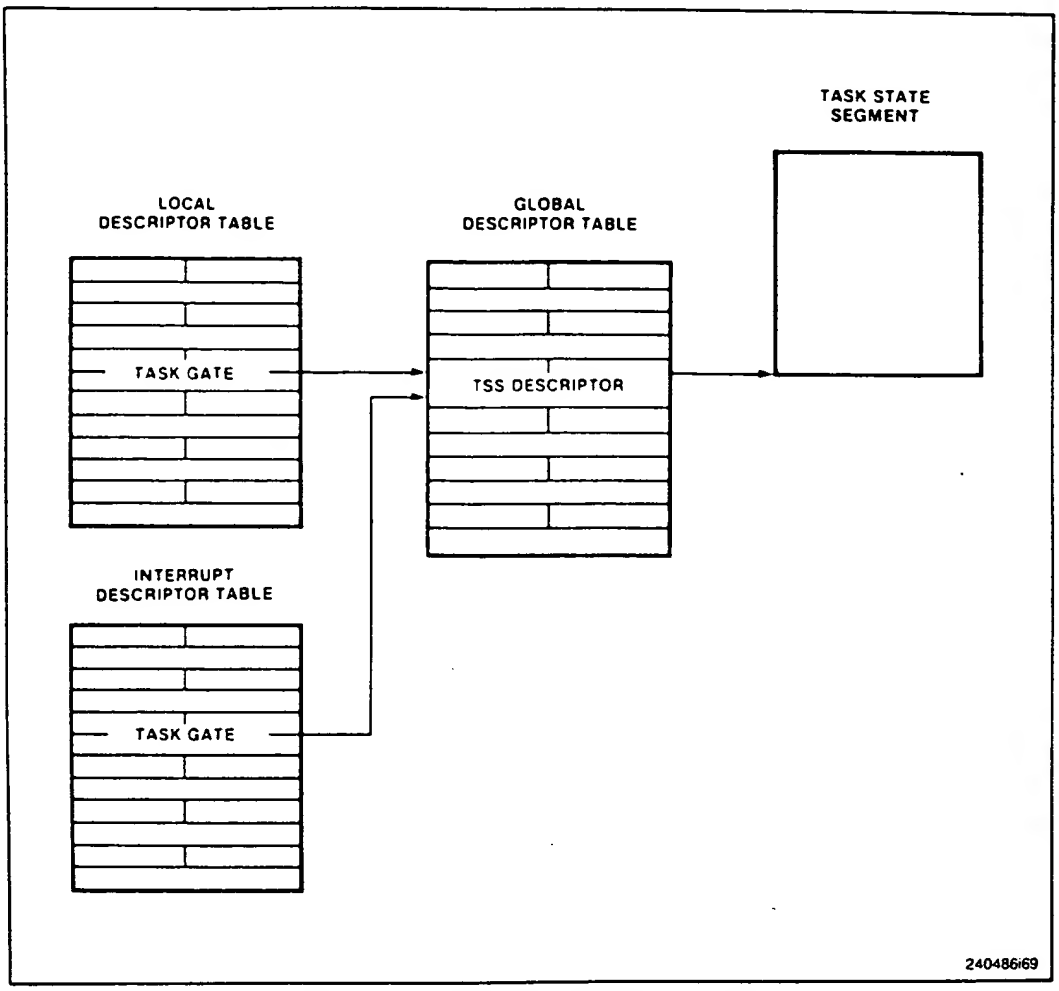


Figure 7-5. Task Gates Reference Tasks

An interrupt service routine always returns execution to the interrupted procedure, which may be in another task. If the NT flag is clear, a normal return occurs. If the NT flag is set, a task switch occurs. The task receiving the task switch is specified by the TSS selector in the TSS of the interrupt service routine.

A task switch has these steps:

1. Check that the current task is allowed to switch to the new task. Data-access privilege rules apply to JMP and CALL instructions. The DPL of the TSS descriptor and the task gate must be greater than or equal to both the CPL and the RPL of the gate selector. Exceptions, interrupts, and IRET instructions are permitted to switch tasks regardless of the DPL of the destination task gate or TSS descriptor.

Fig. 1 D: PRIOR ART

Fig. 2

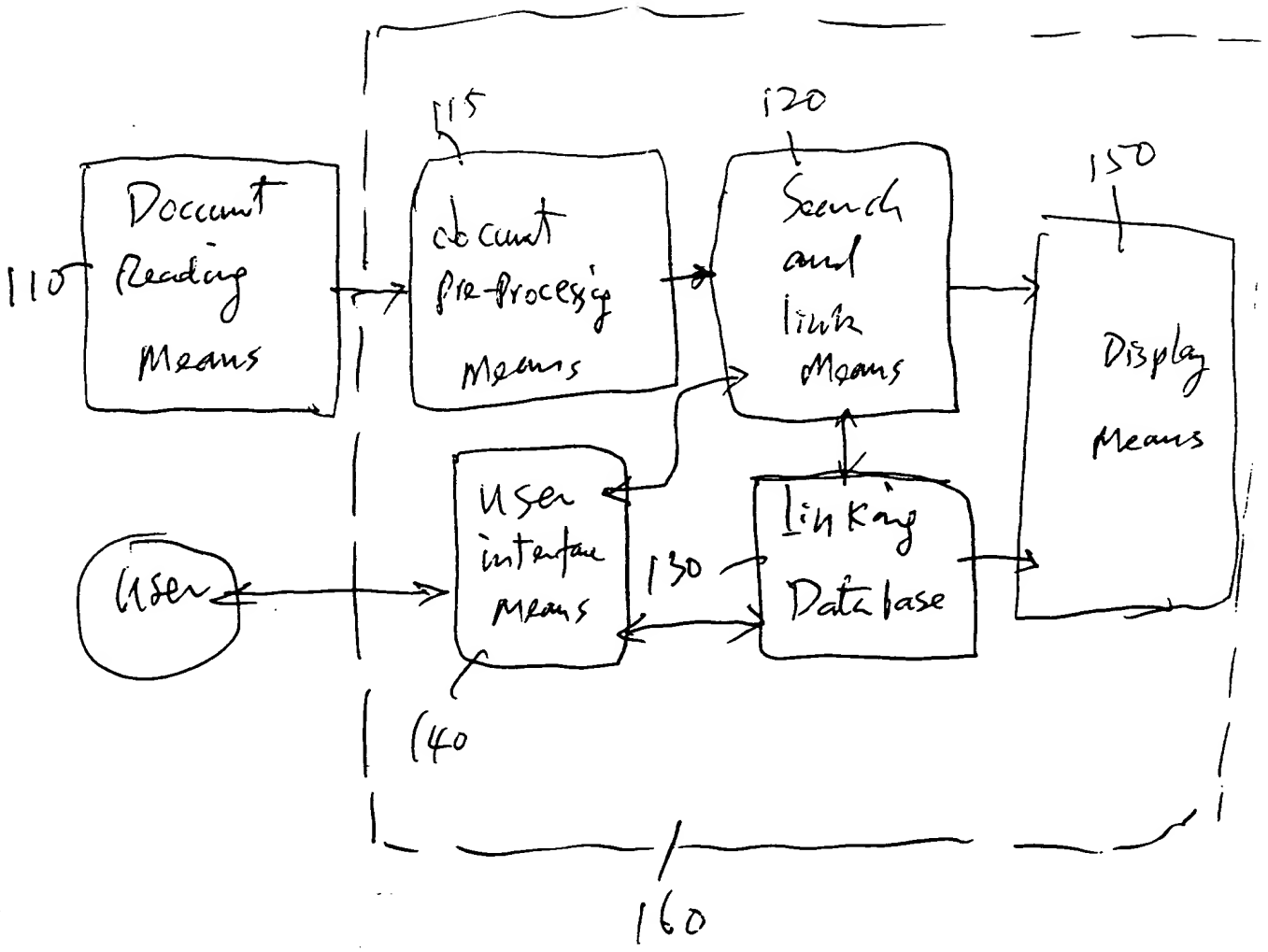
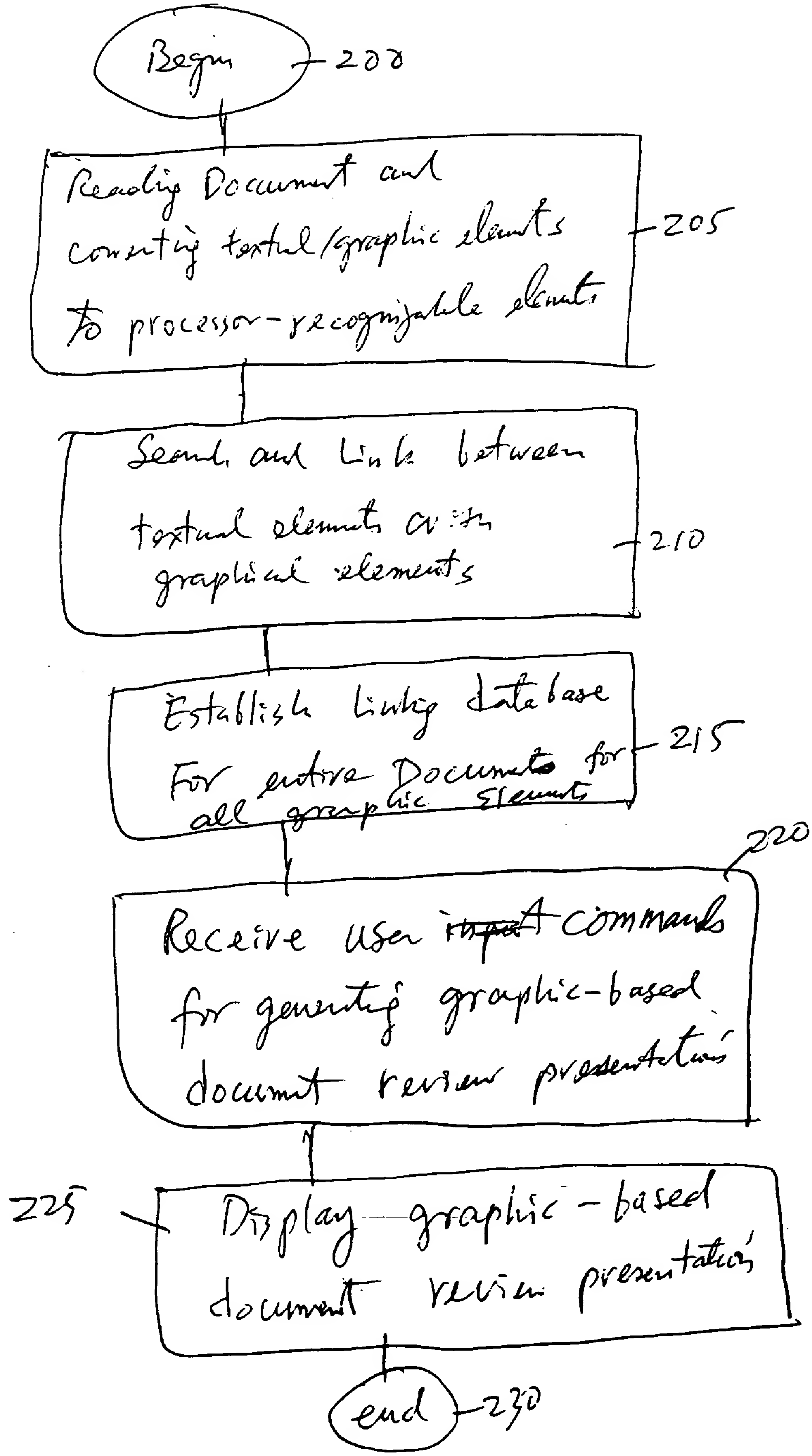

Document Reading Means
110
document pre-processing Means
115
Search and link Means
120
Display Means
150
User interface means
User
130
Linking Database
140
160

Fig. 3


Begin
200
Reading Document and converting textual/graphic elements to processor-recognizable elements
205
Search and Link between textual elements with graphical elements
210
Establish linking database for entire Documents for all graphic Elements
215
Receive user ~~input~~ commands for generating graphic-based document review presentation
220
225
Display graphic-based document review presentation
end
230

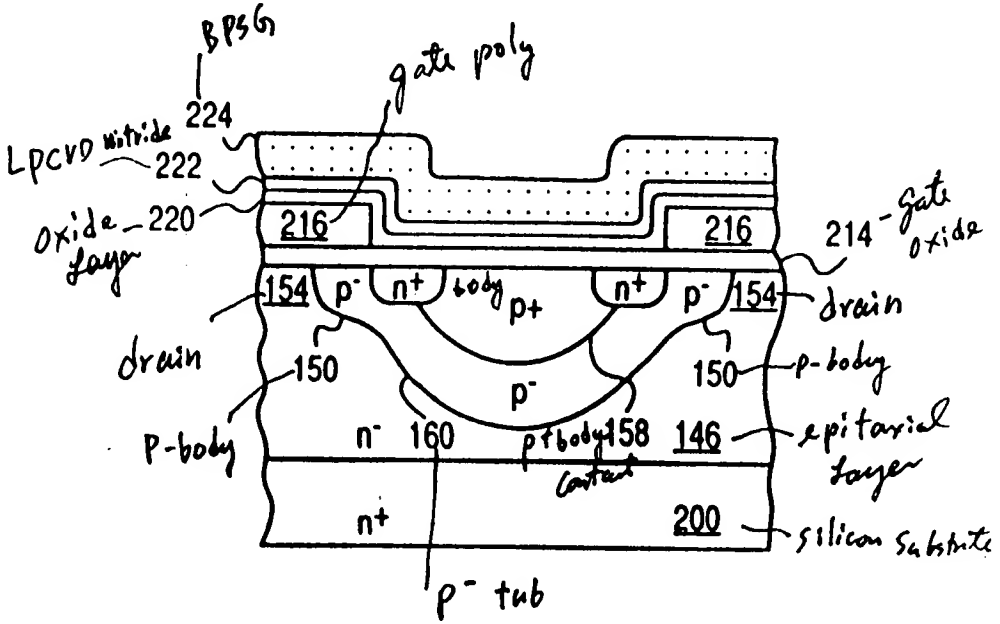


FIG. 16A

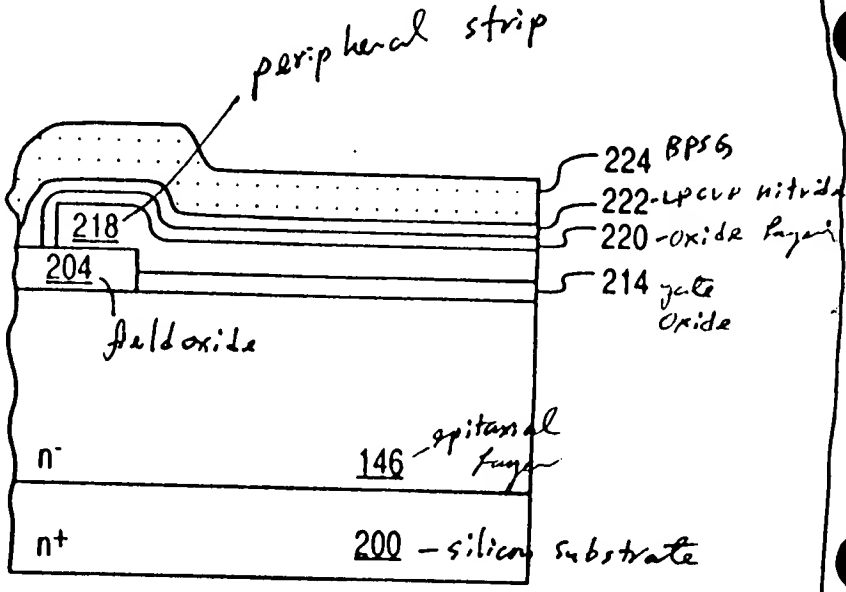


FIG. 16B

Fig. 4A.- Every Graphic Element Shown with Numerical

Fig. 4B Naming Term BPSG shown with Textual Description Box

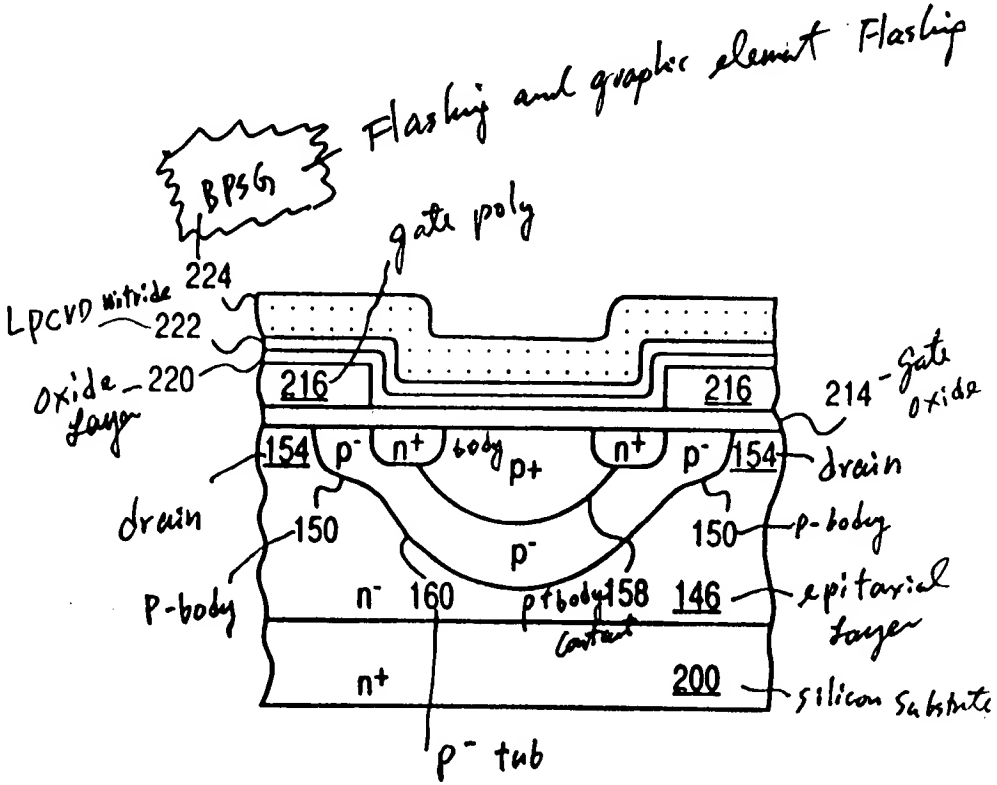


FIG. 16A

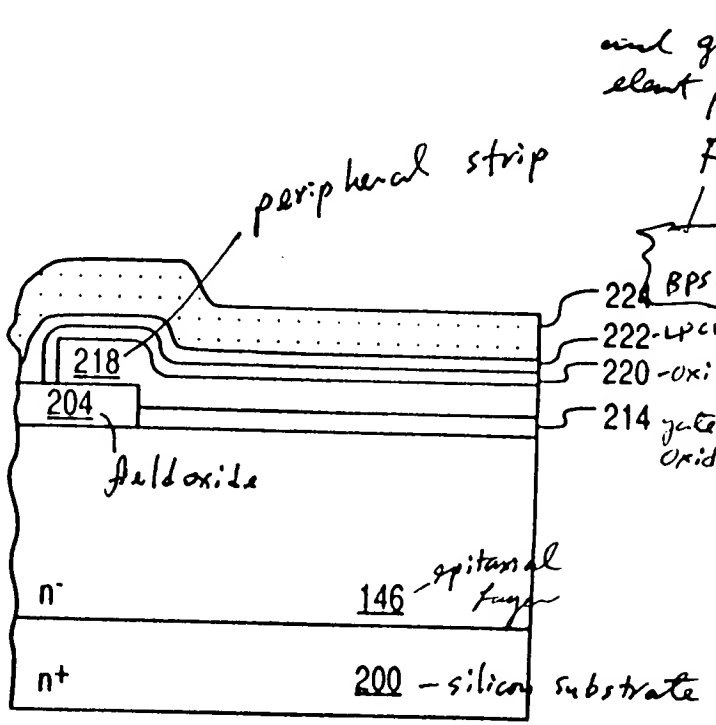


FIG. 16B

Textual Description Box

Naming term : BPSG

col. 5, lines 50-54 The device is completed by depositing (optionally) about 1000 Angstroms of LPCVD nitride 222 followed by a BPSG deposition of about 0.8-1.3 microns and a BPSG reflow 224 at about 850-1000 degrees C (FIG. 16)

Fig. 4 Co: Naming Term BPSG. Shown with Multiple Drawings With Naming Term Flashing and graphic element Flashing

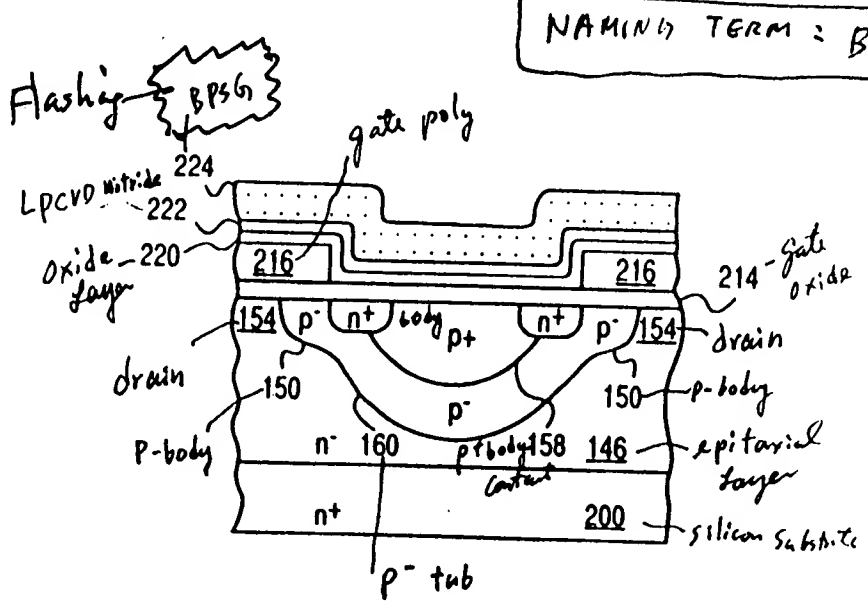


FIG. 16A

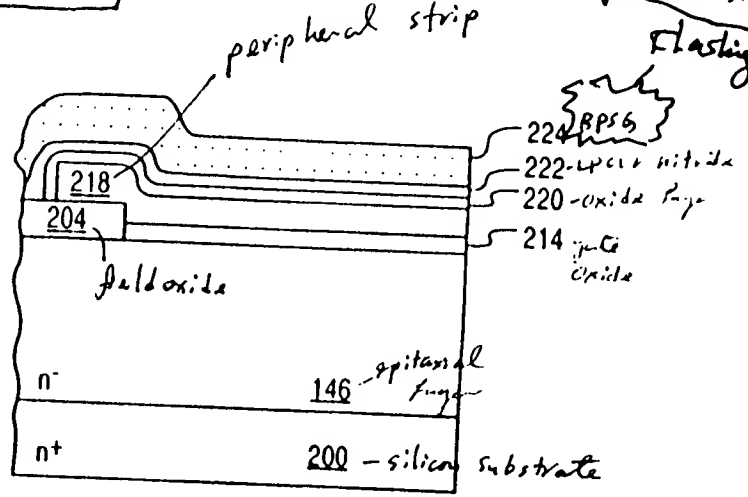


FIG. 16B

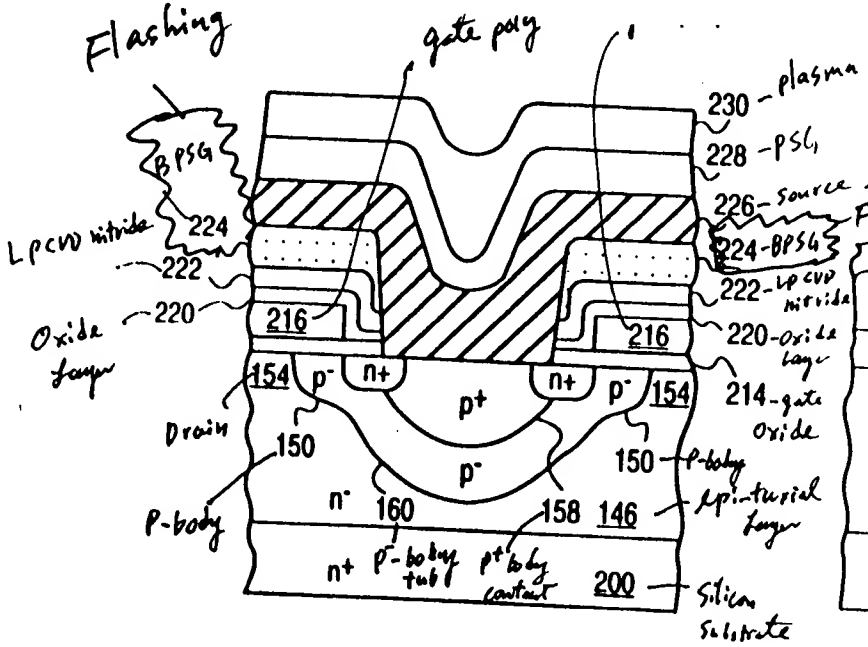


FIG. 17A

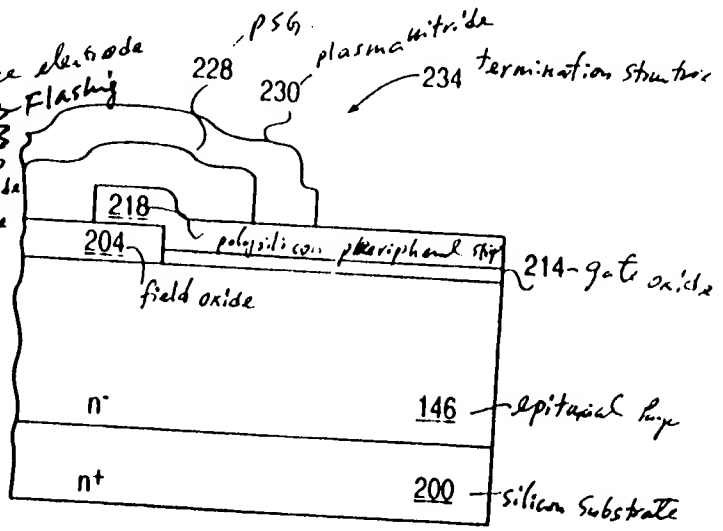


FIG. 17B